Secondment report

TIRAMISU DC1.1

Fellow:	Ashwin Santhosh
Research project title:	“Reliable RISC-V based Architectures for Edge AI”
From:	TUT
To:	IFAG
Secondment period:	13.04.2026 – 30.04.2026 (18 days)

Activities during the secondment

Scope and objectives

1. Further develop and automate the fault localization approach established during the previous secondment.
2. Gain further practical experience with Infineon’s verification, fault injection, and simulation environment.
3. Complete the experimental evaluation and prepare the research results for publication.

Activities

1. Automated the SBST fault localization flow, including runtime identification of fault-detecting patterns and post-processing for ranked fault narrowing.
2. Performed fault injection experiments using Infineon's internal automation flow and Cadence Xcelium in collaboration with the IFAG team.

Main results achieved

1. Achieved 100% identification of fault-detecting SBST patterns and reduced the fault candidate space by over 96% on average, with exact identification for 48% of detectable faults.
2. The joint paper *“Runtime Pattern Identification and Ranked Fault Narrowing in SBST for RISC-V Processors”* was submitted to DFTS 2026 (subsequently accepted).

Next steps

1. Present the accepted work at DFTS 2026
2. Extend and evaluate the proposed fault localization approach on additional RISC-V processor components.

Self-evaluation

Overall score

I consider this secondment successful, with regards to the research objectives achieved, skills developed, supervision quality, diversity of the resources. (Agree = 5 … Disagree = 1)

Agree - 5

Optional comments

None

Date of the report approval by the supervisor: 04.09.2026

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