TIRAMISU

Funded by
the European Union

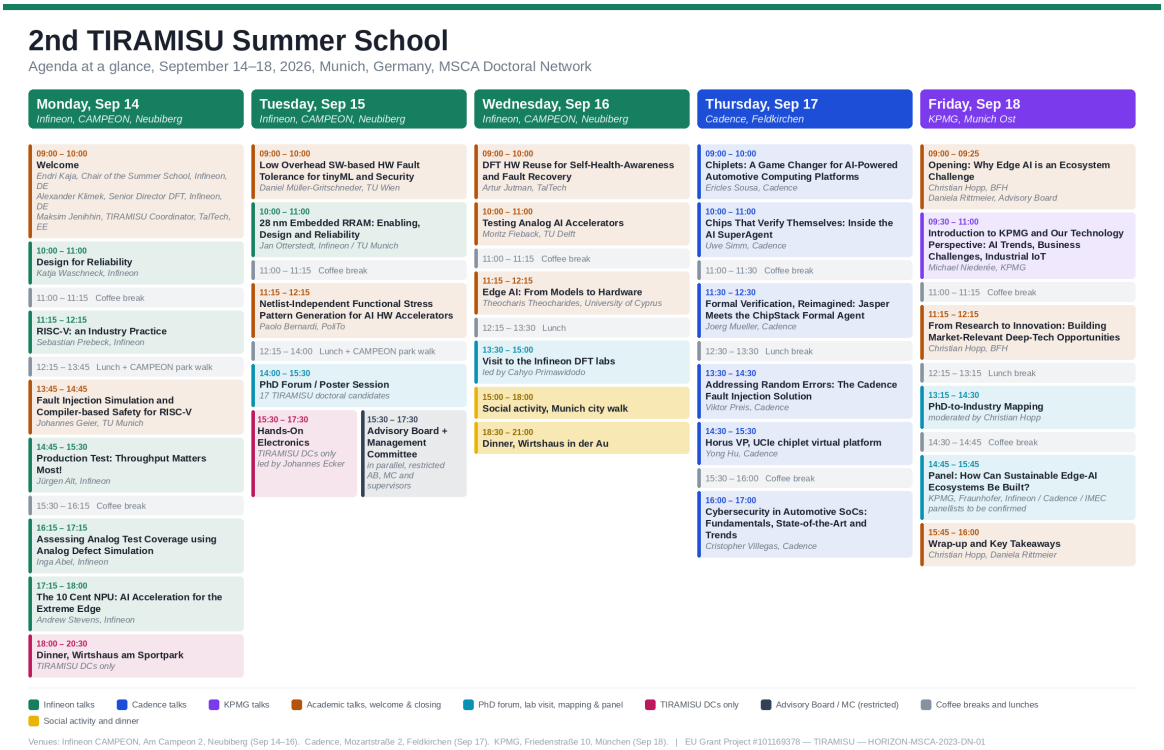
2nd TIRAMISU Summer School

“From Reliable Edge-AI Silicon to Scalable Deep-Tech Ecosystems”

September 14-18, 2026, Munich, Germany
Hosted by Infineon Technologies, Cadence Design Systems and KPMG

The 2nd **TIRAMISU** Summer School is the industry-led edition of the network's annual training week, and for once the doctoral candidates spend it inside the companies rather than in a lecture hall. Three hosts share the week. Infineon Technologies opens at its CAMPEON campus in Neubiberg with three days on design for reliability, RISC-V in industrial practice, production test, analog defect simulation and NPUs for the extreme edge, mixing Infineon speakers on the first day with talks from the **TIRAMISU** partner universities on the following two. Cadence Design Systems takes Thursday in Feldkirchen: chiplets, agentic verification, formal, fault injection and automotive cybersecurity. KPMG closes the week at Friedenstraße with an Industry & Innovation Day built around the project's WP4 topics, where each PhD project gets mapped onto an industrial use case and a panel asks what a sustainable European Edge-AI ecosystem actually requires.

Around the talks sit a visit to the Infineon DFT labs, a hands-on electronics session, a poster forum with all doctoral candidates, and a city walk through Munich. Participation is restricted to the **TIRAMISU** consortium and invited guests.



Chair of the Summer School

- **Endri Kaja**, Infineon Technologies, Germany

Organizing Committee

- **Endri Kaja** and **Wolfgang Ecker**, Infineon Technologies, Germany
- **Ahmet Cagri Bagbaba** and **Ericles Sousa**, Cadence Design Systems, Germany
- **Christian Hopp** and **Branka Hadji Misheva**, Bern University of Applied Sciences, Switzerland

TIRAMISU Project Coordination

- **Maksim Jenihhin**, Tallinn University of Technology, Estonia

Programme

Monday, September 14

Host: Infineon Technologies, CAMPEON, Neubiberg, Infineon speakers

09:00 - 10:00 Welcome
Endri Kaja (Chair of the Summer School), Infineon Technologies, DE
Alexander Klimek (Senior Director DFT), Infineon Technologies, DE
*Maksim Jenihhin (**TIRAMISU** Coordinator), TalTech, EE*

10:00 - 11:00 Design for Reliability
Katja Waschneck, Infineon Technologies, DE

11:00 - 11:15 Coffee break

11:15 - 12:15 RISC-V: an Industry Practice
Sebastian Prebeck, Infineon Technologies, DE

12:15 - 13:45 Lunch break + CAMPEON park walk

13:45 - 14:45 Fault Injection Simulation and Compiler-based Safety and Security Countermeasures for RISC-V
Johannes Geier, TU Munich, DE

14:45 - 15:30 Production Test: Throughput Matters Most!
Jürgen Alt, Infineon Technologies, DE

15:30 - 16:15 Coffee break

16:15 - 17:15 Assessing Analog Test Coverage using Analog Defect Simulation
Inga Abel, Infineon Technologies, DE

17:15 - 18:00 The 10 Cent NPU: AI Acceleration for the Extreme Edge
Andrew Stevens, Infineon Technologies, DE

18:00 - 20:30 Dinner
***TIRAMISU** DCs only, Wirtshaus am Sportpark*

Tuesday, September 15

Host: Infineon Technologies, CAMPEON, Neubiberg, project partners

09:00 - 10:00 Low Overhead SW-based HW Fault Tolerance for tinyML and Security Applications
Daniel Müller-Gritschneder, TU Wien, AT

10:00 - 11:00 28nm Embedded RRAM for Consumer and Industrial Products: Enabling, Design, and Reliability
Jan Otterstedt, Infineon Technologies / TU Munich, DE

11:00 - 11:15 Coffee break

11:15 - 12:15 Netlist-Independent Functional Stress Pattern Generation Strategy for AI HW Accelerators Embedded into Automotive SoCs
Paolo Bernardi, PoliTo, IT

12:15 - 14:00 Lunch break + CAMPEON park walk

14:00 - 15:30 PhD Forum / Poster Session by TIRAMISU DCs

- *DC1.1-TUT* — **Ashwin Santhosh**, “Reliable RISC-V based Architectures for Edge AI”
- *DC1.3-TUD* — **Chayma Amaaz**, “Analog in-memory brain-inspired edge processors for Edge AI”
- *DC1.4-IFAG* — **Michael Elias**, “Detection and recovery reliability mechanisms for digital edge AI devices”
- *DC1.5-IFAG* — **Zishu Chai**, “Detection and recovery mechanisms for analog edge AI hardware”
- *DC2.1-DUS* — **Germano Berto Girondi**, “Virtual Prototyping as Hardware-Software Co-Design Methodology for Next-Generation Automotive Edge-AI”
- *DC2.2-PDT* — **Gustavo Vilar de Farias**, “Reliability estimation techniques for AI accelerators”
- *DC2.3-CDNS* — **Sergiu-Mohamed Abed**, “Analysis and improvement of fault tolerance and safety of AI accelerators”
- *DC2.4-CDNS* — **Dwijesh Kurada**, “Development of high-level fault models for validation of AI accelerators”
- *DC3.1-UCY* — **Dimitrios Stylianos Lampridis**, “Efficient and robust hardware neural network model accelerators for Edge AI”

- *DC3.2-UCY* — **Yobsan Bayisa Leta**, “Robustification of dynamic neural networks via contextual awareness and attention for edge AI”
- *DC3.3-PDT* — **Aobo Cui**, “Software-based hardening solutions for AI-based architectures”
- *DC3.4-TUT* — **Hafsa Tanveer**, “Neural Architecture Search framework for efficient and reliable hybrid CNN-Transformer models for Edge AI”
- *DC3.5-TUD* — **Illiana Khalida Binti Mohd Shukri**, “Reliability-aware mapping and optimization techniques for Edge AI”
- *DC4.1-BFH* — **Benedek Fülöp**, “Human Oversight and Innovation Management for Edge AI R&D&I Ecosystems”
- *DC4.2-BFH* — **Xiangrui Zeng**, “Case Study of Innovation Management for Edge AI Hardware Design Flow”

15:30 - 17:30 Hands-On Electronics
TIRAMISU *DCs only, led by Johannes Ecker*

15:30 - 17:30 Advisory Board and Management Committee Meetings
in parallel; restricted

- **Daniela Rittmeier**, Advisory Board, Capgemini, DE
- **Daniel Müller-Gritschneder**, Advisory Board, TU Wien, AT
- **Davide Appello**, Advisory Board, Technoprobe, IT
- **Francky Catthoor**, Advisory Board, NTUA, GR
- ***TIRAMISU*** *Management Committee members and supervisors*

Wednesday, September 16

Host: Infineon Technologies, CAMPEON, Neubiberg, project partners

09:00 - 10:00 DFT HW Reuse for Self-Health-Awareness and Fault Recovery in a Multicore CPU Subsystem
Artur Jutman, Tallinn UT, EE

10:00 - 11:00 Testing Analog AI Accelerators
Moritz Fieback, TU Delft, NL

11:00 - 11:15 Coffee break

11:15 - 12:15 Edge AI: From Models to Hardware
Theocharis Theocharides, University of Cyprus, CY

12:15 - 13:30 Lunch

13:30 - 15:00 Visit to the Infineon DFT labs
Led by DFT expert Cahyo Primawidodo, Infineon Technologies, DE

15:00 - 18:00 Social activity
City walk tour of Munich

18:30 - 21:00 Dinner
Wirtshaus in der Au

Thursday, September 17

Host: Cadence Design Systems, Feldkirchen, Cadence speakers

09:00 - 10:00 Chiplets: A Game Changer for AI-Powered Automotive Computing Platforms
Ericles Sousa, Cadence Design Systems, DE

10:00 - 11:00 Chips That Verify Themselves: Inside the AI SuperAgent
Uwe Simm, Cadence Design Systems, DE

11:00 - 11:30 Coffee break

11:30 - 12:30 Formal Verification, Reimagined: Jasper Meets the ChipStack Formal Agent
Joerg Mueller, Cadence Design Systems, DE

12:30 - 13:30 Lunch break

13:30 - 14:30 Addressing Random Errors: The Cadence Fault Injection Solution
Viktor Preis, Cadence Design Systems, DE

14:30 - 15:30 Horus VP
Yong Hu, Cadence Design Systems, DE

15:30 - 16:00 Coffee break

16:00 - 17:00 Cybersecurity in Automotive SoCs: Fundamentals, State-of-the-Art and Trends
Cristopher Villegas, Cadence Design Systems, DE

Friday, September 18, Industry & Innovation Day

Host: KPMG, Munich, "From Edge-AI Research to Scalable Deep-Tech Ecosystems"

09:00 - 09:25 Opening: Why Edge AI is an Ecosystem Challenge
Christian Hopp, BFH, CH, and Daniela Rittmeier, Member of the Advisory Board

09:30 - 11:00 Introduction to KPMG and Our Technology Perspective: AI Trends, Business Challenges, and Industrial IoT in Practice
Michael Niederée, KPMG, DE

11:00 - 11:15 Coffee break

11:15 - 12:15 From Research to Innovation: Building Market-Relevant Deep-Tech Opportunities
Christian Hopp, BFH, CH

12:15 - 13:15 Lunch break

13:15 - 14:30 PhD-to-Industry Mapping
Moderated by Christian Hopp, with input from industry and advisory board participants

14:30 - 14:45 Coffee break

14:45 - 15:45 Panel Discussion: How Can Sustainable Edge-AI Ecosystems Be Built?
KPMG, Fraunhofer, Infineon / Cadence / IMEC, Daniela Rittmeier (Capgemini, DE), Davide Appello (Technoprobe, IT). Final list of panellists to be confirmed.

15:45 - 16:00 Wrap-up and Key Takeaways
Christian Hopp and Daniela Rittmeier

Venues and travel

Monday to Wednesday, September 14-16, Infineon CAMPEON

Conference Zone, Building 2, Am Campeon 2, 85579 Neubiberg

- *Start:* Monday at 09:00.
- *Getting there:* take S-Bahn line S3 to Fasanenpark, then walk about 10 minutes to the site.
- *Badges:* all participants are pre-registered at the reception in Building 1 (Am Campeon 1). Collect your badge there each morning and return it at the end of each day. Allow a few extra minutes on Monday for badge pickup.
- *On site:* student assistants Paula and Andro will help you navigate the venue and answer questions.
- *Catering:* coffee breaks and lunches are provided on site throughout the three days.

Thursday, September 17, Cadence Design Systems

Mozartstraße 2, 85622 Feldkirchen

- *From Munich Hauptbahnhof:* take S-Bahn line S2 towards Erding and get off at Feldkirchen.
- *From Feldkirchen station:* walk about 12 minutes to the office, or take Bus 234 towards Unterföhring and get off at Mozartstraße (about 5 minutes).
- *On arrival:* check in at the reception desk on the left. Names are pre-registered for validation.
- *Room:* the workshop is held in the Alexander Graham Bell room.

Friday, September 18, KPMG

KPMG AG Wirtschaftsprüfungsgesellschaft, Friedenstraße 10, 81671 München

- *Getting there:* the office is close to Munich Ostbahnhof, which is served by multiple S-Bahn lines.

A map of all three venues is on the event page: tiramisu-project.eu/events/2nd-tiramisu-summer-school-munich

Questions about any of the venues go to Endri Kaja, Ahmet Cagri Bagbaba or Christian Hopp.

Abstracts and session focuses

Thursday, September 17, Cadence Design Systems

Chiplets: A Game Changer for AI-Powered Automotive Computing Platforms

Ericles Sousa, Cadence Design Systems, DE

Abstract. Recently, MIT Technology Review named chiplets and AI among the Top 10 Breakthrough Technologies. As automotive computing platforms grow in complexity, monolithic SoCs face increasing challenges in scalability, cost, and design flexibility. This keynote explores how chiplet-based architectures, enabled by the UCIe standard, are driving the next generation of AI-powered automotive compute platforms. Through real-world examples, it highlights how chiplets can address functional safety requirements while accelerating the development of scalable autonomous and software-defined vehicles.

Chips That Verify Themselves: Inside the AI SuperAgent

Uwe Simm, Cadence Design Systems, DE

Abstract. ChipStack AI SuperAgent puts AI agents to work as chip design and verification engineers, from understanding the specification through RTL, testbenches, execution and debug. At its core is a Mental Model that acts as the single source of truth, orchestrating specialised agents across Cadence EDA tools. The session walks through the formal, UVM, unit-testing and debug super agents in one end-to-end verification flow, and the results they deliver: verification cycles shrinking from weeks to hours, twice as many bugs caught, with on-premises deployment that slots into existing flows without disruption. A live demo of ChipStack in action will follow if time permits.

Formal Verification, Reimagined: Jasper Meets the ChipStack Formal Agent

Joerg Mueller, Cadence Design Systems, DE

Abstract. Formal verification systematically explores design behaviour to find corner-case bugs and prove critical requirements. This session introduces the foundations of formal analysis, including properties, constraints, state-space exploration and proof results, and explains how formal complements simulation. It then explores the breadth of Jasper applications across the chip development flow before showing how Jasper technology is integrated into the ChipStack Formal Agent, bringing proven formal capabilities into an agentic design and verification experience.

Addressing Random Errors: The Cadence Fault Injection Solution

Viktor Preis, Cadence Design Systems, DE

Abstract. Addressing random errors plays a major role in the safety analysis of ASIC designs, for example in calculating diagnostic coverage. The nature of random errors is non-functional; hence, they cannot be addressed by purely functional verification methods. This is where fault injection techniques come into play. This presentation will show the Cadence Fault Injection Solution, focusing on diagnostic coverage calculation for random errors with support for both permanent and transient faults.

Horus VP

Yong Hu, Cadence Design Systems, DE

Abstract. This demo showcases a SystemC/TLM-based Virtual Platform using Cadence Helium Digital Twin technology and demonstrates the Shift-Left methodology applied to UCIe chiplet design. The Virtual Platform consists of an ARM-based automotive application processor chiplet and a Tensilica-based Vision/AI accelerator chiplet. The platform is demonstrated with an example computer vision application. Linux OS is booted in the ARM chiplet and runs applications, for example Python. Data is transferred through UCIe interfaces to the Tensilica chiplet, which employs VQ8 processors for image processing and NEO NPUs for AI applications.

Cybersecurity in Automotive SoCs: Fundamentals, State-of-the-Art and Trends

Cristopher Villegas, Cadence Design Systems, DE

Abstract. Modern cyber-physical systems rely on Functional Safety (FuSa) and Cybersecurity (CS) as two fundamental pillars for ensuring correct and dependable operation. In automotive SoCs, CS has become a critical concern, as malicious attacks can alter system functionality, compromise data integrity, and ultimately lead to hazardous scenarios. This talk introduces the fundamental concepts of automotive CS based on the ISO/SAE 21434 standard, including threats, vulnerabilities, attack paths, risk assessment, and security controls. The relationship between CS and FuSa will be discussed, highlighting parallels and differences with established FuSa concepts. The presentation reviews the current state of the art, including recent research and emerging methodologies for security analysis and validation. An open-source platform example will illustrate practical approaches. The talk concludes with key challenges shaping CS, including the role of Agentic AI in the automotive product lifecycle.

Friday, September 18, KPMG Industry & Innovation Day

Opening: Why Edge AI is an Ecosystem Challenge

Christian Hopp, BFH, CH, and Daniela Rittmeier, Member of the Advisory Board

Framing the day: **TIRAMISU** as a deep-tech ecosystem connecting reliable Edge-AI research, industrial adoption, innovation, and ecosystem development.

Introduction to KPMG and Our Technology Perspective

Michael Niederée, KPMG, DE

A 90-minute session on AI scaling, data strategy, governance, alliances, and the transition from pilots to industrial deployment.

From Research to Innovation: Building Market-Relevant Deep-Tech Opportunities

Christian Hopp, BFH, CH

Input on how research can be translated into innovation opportunities, industrial value propositions, and pathways towards market adoption.

PhD-to-Industry Mapping

Moderated by Christian Hopp, with input from industry and advisory board participants

Interactive workshop in which the doctoral candidates translate their research projects into industrial use cases, value propositions, data requirements, ecosystem roles, scaling barriers, and business readiness.

Panel Discussion: How Can Sustainable Edge-AI Ecosystems Be Built?

KPMG, Fraunhofer, Infineon / Cadence / IMEC, Daniela Rittmeier (Capgemini, DE), Davide Appello (Technoprobe, IT). Final list of panellists to be confirmed.

Discussion on ecosystem orchestration, industrial scaling, safety and governance, data readiness, partner roles, and the transition from research to industrial adoption.